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Anticipation and Mitigation of Conducted emissions in a Dc-Dc Buck converter Using LTspice

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Abstract: EMI (electromagnetic interference) is unwanted electromagnetic energy that could disturb the proper working of a device under its influence. The EMC (electromagnetic compatibility) test is taken very late in the design cycle when there is very little chance of modification left in the DUT (device under test). Motivated by the challenge, this report presents the idea that could predict the conducted emissions emanating from the DUT in LTspice simulation software before they happen in real word circuit, that way, we could not only save the development time but as well as the cost of development. The focus is to study the EMI behavior of dc-dc step-down or buck converter (case study) since it is a rich source of EMI. A lot of work has been placed on designing buck converter while referring to the datasheets and modeling the parasitic components such as ESL (equivalent series inductance), ESR (equivalent series resistance) of the output capacitor using an online database called as RedExpert. The emission due to electric field coupling (parasitic capacitive effect) is also considered. The simulation results obtained using LTspice were accurate enough to be comparable with the experimental measurements performed at the Laboratory of Wurth Elektronik.

Keywords: EMI, EMC, Modeling parasitic components, Buck converter, LTspice, RedExpert

I. INTRODUCTION

This With the advancement in electronics, the devices are further shrinking in sizes and therefore, are getting more and more closer to each other as proposed by Moore's Law [1]. Thus, the problem of EMI is getting more and more attention. The EMI emanating from a device could not only disturb the proper functioning of another device held in its proximity but could also liable to be influenced by that device itself. Therefore, the design engineers need to mitigate these emissions to a level that is acceptable as per different regulations such as CISPR (Comité International Spécial des Perturbations Radioélectriques), FCC (Federal Communication Commission), EU (European Union), and many other EMC regulations implemented and followed worldwide [2]. These EMC standards have forced limits on the amount of electromagnetic interference noise that the converters will inject into the commercial supplies [3].

The EMC tests are taken very late in the development cycle of a device when there is little chance of modification left in the device itself [4]. Another problem concerning EMC is identifying which component, i.e., Common mode and Differential mode, of noise is dominant over the other [5]. Based on the type of noise certain filtering techniques are implemented to suppress the EMI.

To tackle these problems, this article presents the idea of modeling and simulating the conducted emissions emanating from a DUT (Buck converter in our case) in LTspice. Buck converter is a device that is used to step down an input dc voltage level to the desired output dc voltage. These converters are very efficient in the context of working efficiency, compact sizes, and lightweight. The major problem, however, with buck converters is that these work on the high switching frequency and the square pulse associated with it could cause EMI in the device [6]. We could anticipate the conducted EMI in buck converter by properly modeling the parasitic elements of the passive components used in buck converters such as capacitor, inductor, and resistor. Another major contribution to conducted emissions or more specifically the CM (Common mode) emissions is due to electric field coupling (also known as parasitic capacitive coupling).

We modeled the ESL and ESR of the output capacitor using an online database software known as RedExpert that contains all the datasheets of the passive components, manufactured by Wurth Elektronik. The electric field couplings between the high switching dv/dt node and GRP (ground reference plane) and casing of the device connected to the buck converter and GRP are modeled and replaced by simple parallel plate capacitors (stray capacitance) in LTspice.

After establishing the whole setup in LTspice circuit simulation software, the simulation results are compared with the experimental result performed at the laboratory

of Wurth Elektronik. Fig. 1 shows the experimental setup of the EMC test at Wurth Elektronik.

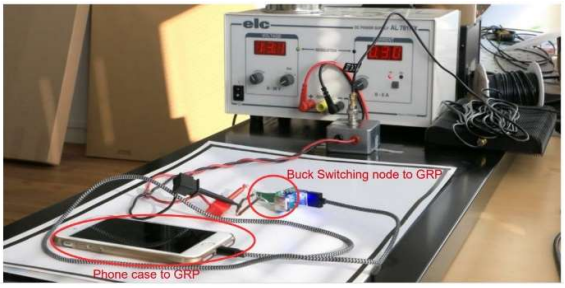

Fig. 1 EMC experimental test setup at Wurth Elektronik

After validation of results, a technique is also implemented to split the components of conducted emissions into common mode and differential mode. The emissions are compared to a standard limit line added to LTspice through plot settings and based on that different built-in filters are used to mitigate the noise.

In this project, we have modeled a buck converter while referring to the datasheet provided by the manufacturer. The LT3975 model of the buck converter is used in LTspice for simulation. Fig 2 shows the circuit diagram of the LT3975 buck converter.

II. METHODOLOGY

A. Buck Converter

In this project, we have modeled a buck converter while referring to the datasheet provided by the manufacturer. The LT3975 model of the buck converter is used in LTspice for simulation. Fig 2 shows the circuit diagram of the LT3975 buck converter.

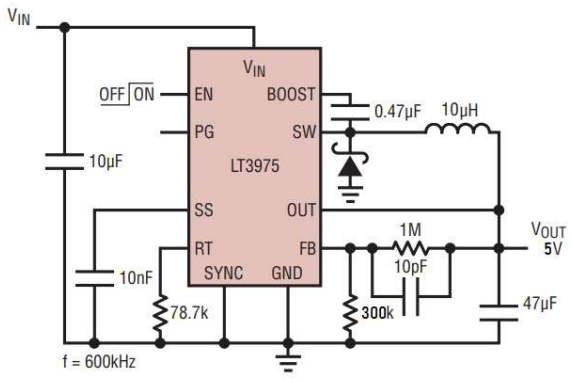

Fig. 2 LT3975 Buck converter

The equations used for modeling different parameters of the LT3975 buck converter are mentioned below:

$$R_T = \frac{5.51}{(f_{sw})^{1.09}} - 9.27 \quad (1)$$

$$R_1 = R_2\left(\frac{V_{out}}{1.197\,V} - 1\right) \quad (2)$$

$$L = \frac{V_{out} + V_d}{1.5 \times f_{sw}} \quad (3)$$

$$C_{out} = \frac{200}{V_{out} \times f_{sw}} \quad (4)$$

The parameters selected for the model are listed in table 1.

Table 1 Buck converter parameters

Input voltage	*Output voltage*	*Frequency*	*Load*
14v	5V	600KHz	5Ω

B. Modeling the output capacitor

The parasitic components of the output capacitor are modeled using the RedExpert database. The RedExpert database allows the user to choose the most suitable passive components required for a converter, buck converter in our case. We find the most suitable output capacitor for our application using RedExpert, which is 22 microfarads. The ESR and ESL of that capacitor are determined using the impedance/frequency graph as shown in Fig. 3. The ESR is calculated at the resonance frequency (~666 kiloHertz) where the capacitor acts as a resistor. However, The ESL can be found at the frequency above the resonance; we calculated this value at 100 megaHertz.

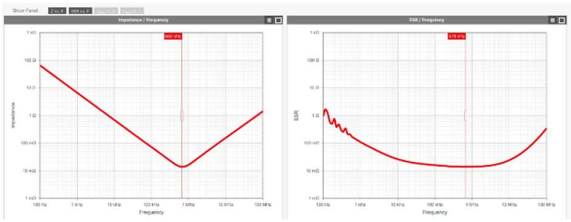

Fig. 3 Impedance/Frequency graph in RedExpert

C. Electric Field Coupling

The first, but major contribution to CM interference in a buck converter is the electric field coupling between the high dv/dt switching node voltage and GRP. Another major contribution that was observed during our project is electric field coupling is the voltage between the metallic casing of the device connected to the DUT and the GRP. This can be modeled and replaced by a simple parallel plate capacitor (Stray capacitance).

D. Wire inductance

The wire inductance can be modeled and represented using the equation [7] shown below:

$$L = 0.0002l\left[l_n\left(\frac{2l}{r}\right) - 0.75\right] \quad (5)$$

E. Line Impedance Stabilization Network

The LISN (Line Impedance Stabilization Network) is one of the major apparatus used during EMC testing of a DUT. For our project, we established the mono-cell topology of LISN [8] which uses the least number of passive components and is used for simulation purposes.

F. EMC Test Setup in LTspice

After modeling all the essential parasitic elements that are necessary for EMC testing. A circuit is developed in LTspice for simulation and validation of results. It is made sure that the circuit, as shown in Fig. 4, resembles the experimental setup performed in Wurth Elektronik (W.E) laboratory for validation.

The standardized limits for this experiment are set according to EN 55105; Class B Conducted, Quasi-Peak. The Plot settings are set to investigate the frequency spectrum from 10 kiloHertz to 30 megaHertz. The EN 55105 is the title of standard for Limits and methods of measurement of radio disturbance characteristics of electrical lighting and similar equipment. [9]

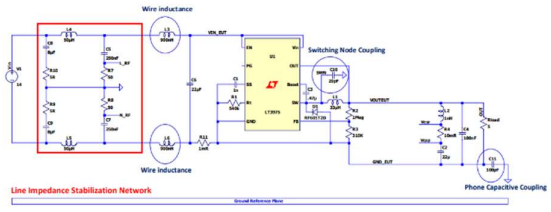

Fig. 4 Simulation circuit developed in LTspice for EMC testing

III. RESULTS

Fig. 5 shows that the frequency spikes of the simulation results in LTspice are matching the experimental results performed at the W.E laboratory.

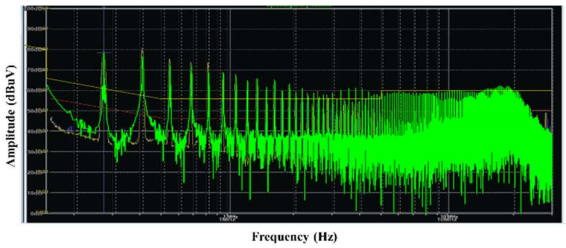

Fig. 5 Comparison between simulation and experimental results

A. Common mode and Differential mode Interference

One of the major issues that EMC engineers face is identifying whether the emissions coming from a DUT have CM interference or DM interference. Based on the mode of noise, a filter is designed for the mitigation of that noise. In practice, a special device is used to decipher the CM interference and DM interference [10]. However, in LTspice, we can achieve this using the mathematical expressions shown below:

$$CM = \frac{V_L + V_N}{2} \quad (6)$$

$$DM = \frac{V_L - V_N}{2} \quad (7)$$

It is observed that the differential mode interference violates the limit lines at lower frequencies. However, the common-mode interference crosses the limit line at higher frequencies, as shown in Fig. 6.

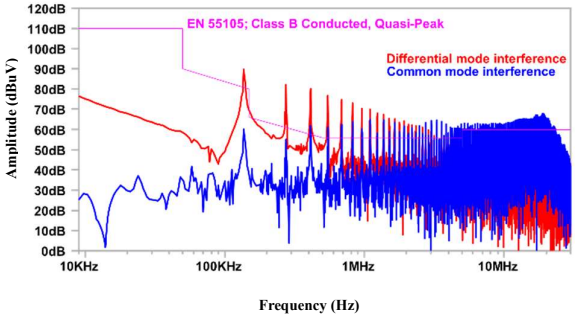

Fig. 6 CM and DM interference

DM interference is suppressed by inserting a de-coupling and noise filtering electrolytic capacitor of 330 microFarads at the input of the buck converter. Fig. 7 shows the effect of the electrolytic capacitor on DM interference. The results are favorable, and the DM interference is mitigated.

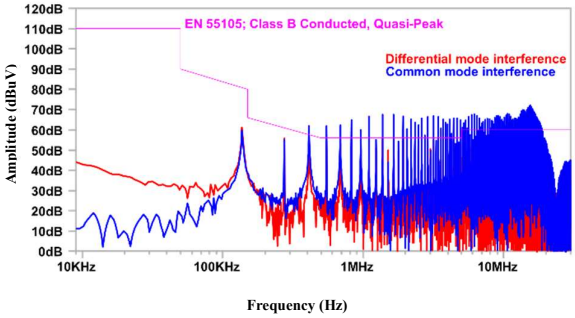

Fig. 7 Effect of Polymer electrolytic capacitor on DM interference

CM interference in a circuit is a bit complex and is hard to filter out using conventional ways of filtering, rather special types of filters are designed in order to

mitigate the CM interference in a circuit. The most commonly used filters to mitigate the CM interference are common mode choke [11]. So, in this report, our work is merely limited to justify our work using common mode choke filters which are already been designed by the professionals. For the sake of validation, we have used a built-in library of model "XS_744821201_1m" for CM chokes provided by Wurth Elektronik. Fig. 8 shows the effect of common-mode choke inserted at the input of buck converter. Both the CM and DM interference are suppressed to a level that is allowed as per the standardized limits.

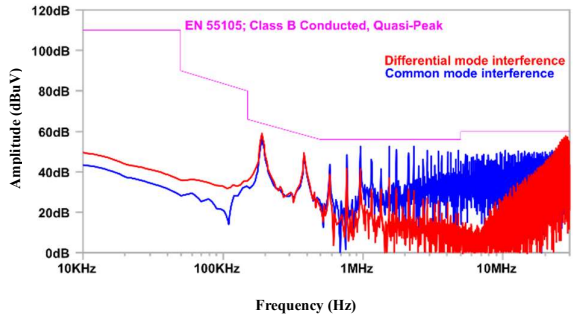

Fig. 8 Effect of Common-mode choke on CM interference

IV. CONCLUSION

We used Buck converter as our case study because it is very efficient when compared with linear converters, however, it is a rich source of unwanted emissions generated due to the high switching frequency components associated with it.

All the simulations are carried out in a circuit simulation software called LTspice. The simulation model of a device can be accurately modeled by inserting lumped elements representing numerous stray and parasitic components of an element. This could make the results taken from simulation correspond a lot better to experimental measurements. Using the same technique, we could effectively pinpoint specific EMI components originating from the equipment under test.

Aside from modeling the parasitic components of a device, it is also important to model electric field capacitive coupling which contributes to common-mode emissions for further accuracy.

Using the technique presented in this report, the design engineers could use LTspice to predict the conducted noise emanating from a device under test, identify which component of the noise is dominant, compare the noise with a standardized limit line set according to the application, and also suppress the noise by adding filters in the circuit. Implementing this technique could save both the development time as well as the cost of the product.

V. ACKNOWLEDGMENT

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